

Application No.: 10/549,291

REMARKS

In response to the Office Action dated January 24, 2008, Applicants have amended claims 1, 4, and 6. Claim 5 has been cancelled, and claims 9-11 have been withdrawn. Support for present amendments may be found in the application at, for example, page 11, line 5 to page 13, line 11 and FIGS. 1 and 11(a)-11(c). Care has been taken to avoid the introduction of new matter. Favorable reconsideration of the application in light of the following comments is respectfully solicited.

Drawings

The drawings were objected to under 35 C.F.R. 1.83(a) for failing to show the semiconductor FIN having a convex shape as described in the specification. Applicants respectfully submit that the rejection is moot in view of the foregoing amendment cancelling claim 5, which recited "...the semiconductor FIN is formed so as to have a convex shape." Withdrawal of this objection is, therefore, respectfully solicited.

Claim Rejections Under 35 U.S.C. § 102

Claims 1, 2, and 4 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent Number 4,996,574 ("Shirasaki"). Applicants traverse this rejection because Shirasaki, at a minimum, fails to describe or suggest a semiconductor device that includes, among other features, a gate electrode extending over the semiconductor substrate from the upper surface of the semiconductor FIN toward both sides of the semiconductor FIN in the shape of a rod, and formed directly on the gate insulating film, as recited in claim 1.

Application No.: 10/549,291

Shirasaki discloses a semiconductor FIN buried in a trench and a gate insulating film formed over sides and the top of the semiconductor FIN. *See e.g.*, Shirasaki at FIGS. 10 and 10A. Shirasaki also discloses a gate electrode of polysilicon, which is deposited on the gate insulating film and extends along the surface of the substrate defining the bottom of the alleged trench and upwardly on the vertical side wall of the alleged trench. *See e.g.*, Shirasaki at col. 7, lines 55-60. As such, the gate electrode of Shirasaki has a concave/convex shape repeated in the gate width direction and does not have a rod shape.

Accordingly, Shirasaki does not describe or suggest a gate electrode extending over the semiconductor substrate from the upper surface of the semiconductor FIN toward both sides of the semiconductor FIN in the shape of a rod, and formed directly on the gate insulating film, as recited in claim 1.

The distinction is important because the gate electrodes having a concave/convex structure, such as the gate electrode of Shirasaki may have high resistance if made thin and may not be able to properly cover the corners with the gate electrode material. If made thick, however, such gate electrode requires larger trench dimensions in the gate width direction; as a result, the transistor becomes large in size.

In contrast, in the present application, the gate electrode extends in the shape of a rod. Accordingly, it is possible to greatly downsize the trench in the gate width direction. Due to this structure, it is also possible to make the gate electrode with sufficient thickness. As a result, the gate resistance can be reduced.

For at least the foregoing reasons, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 1, along with its dependent claims.

Application No.: 10/549,291

Claim Rejections Under 35 U.S.C. § 103

Claims 6 and 8 were rejected under 35 U.S.C. 103(a) as being unpatentable over Shirasaki in view of U.S. Patent Number 6,025,628 ("Lee") and further in view of U.S. Patent Number 7,163,851 ("Abadeer"). Claim 6 has been amended to include features similar to the above-recited features of claim 1. Applicants respectfully submit that Lee and Abadeer do not appear to remedy the shortcomings of Shirasaki to describe or suggest the above-recited features of claim 1. Lee shows a FET semiconductor device and not a FINFET device. As such, the FET of Lee is considerably different from the claimed semiconductor device in structure. Abadeer was only relied upon for an alleged teaching of forming two field-effect transistors on the same substrate. As such, it does not appear that the proposed addition of subject matters from Lee and Abadeer remedies the shortcomings of Shirasaki to describe or suggest the above-recited features of claim 1. For the foregoing reasons and the reasons presented above with respect to claim 1, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 6.

Conclusion

In view of the above amendments and remarks, Applicants submit that this application should be allowed and the case passed to issue. If there are any questions regarding this Amendment or the application in general, a telephone call to the undersigned would be appreciated to expedite the prosecution of the application.

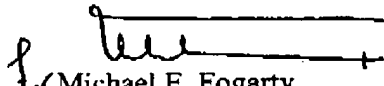
Application No.: 10/549,291

APR 24 2008

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

 (Limited Recognition No. L0250)
f. Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF/LAK:mjb
Facsimile: 202.756.8087
Date: April 24, 2008

**Please recognize our Customer No. 53080
as our correspondence address.**